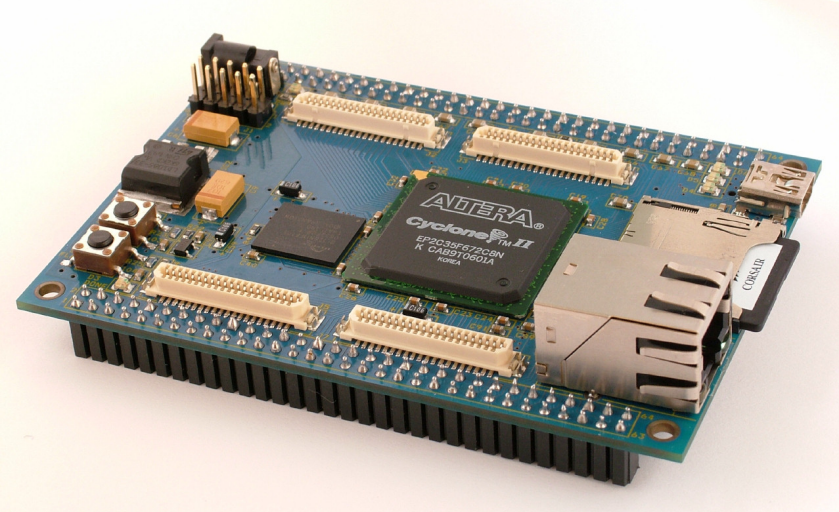
Altera Cyclone II FPGA board

User Manual



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Content

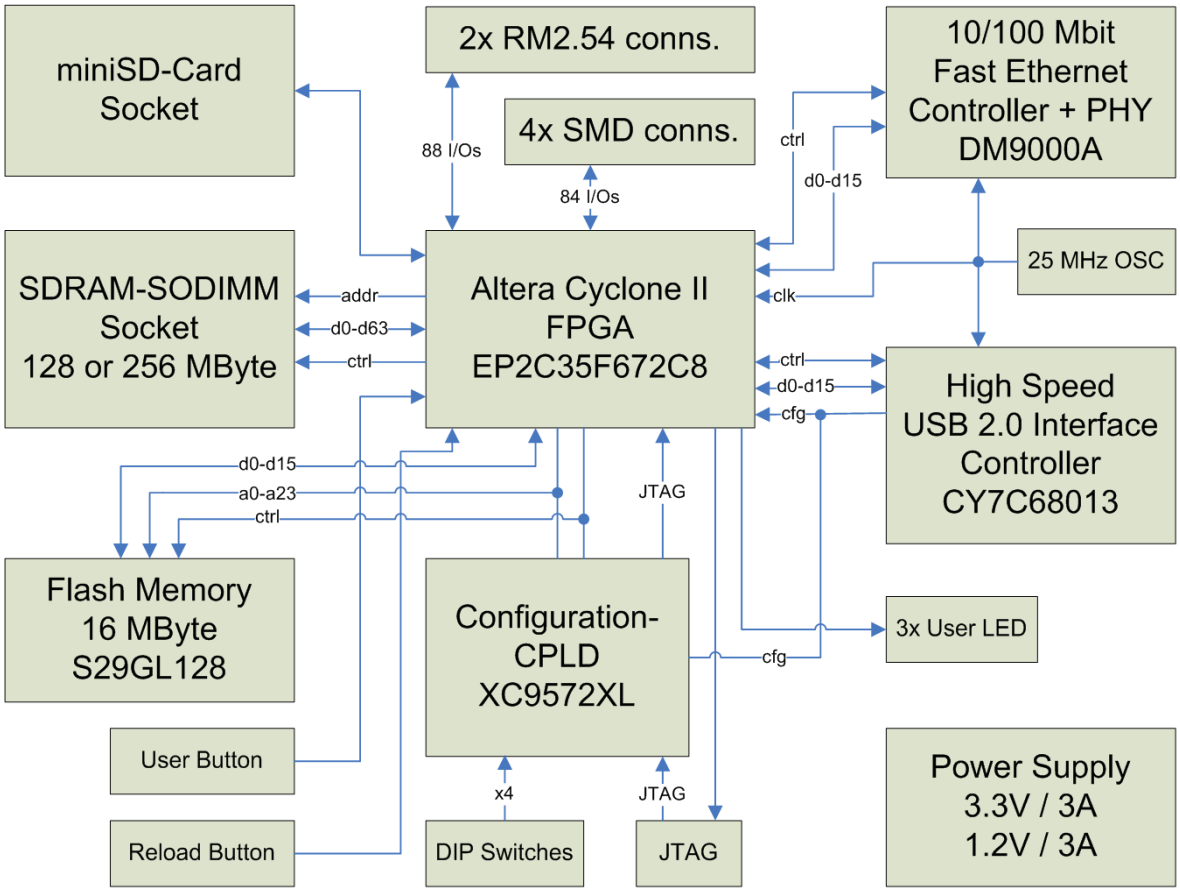
Introduction

Thank you for your interest in Cyclone II based FPGA board! This development board for an experienced user combines many powerful features at very fair price. The possible application range covers stand alone experiments on the one side and operation as a part of a commercial product on the other side. Features make this FPGA board unique among other development boards are:

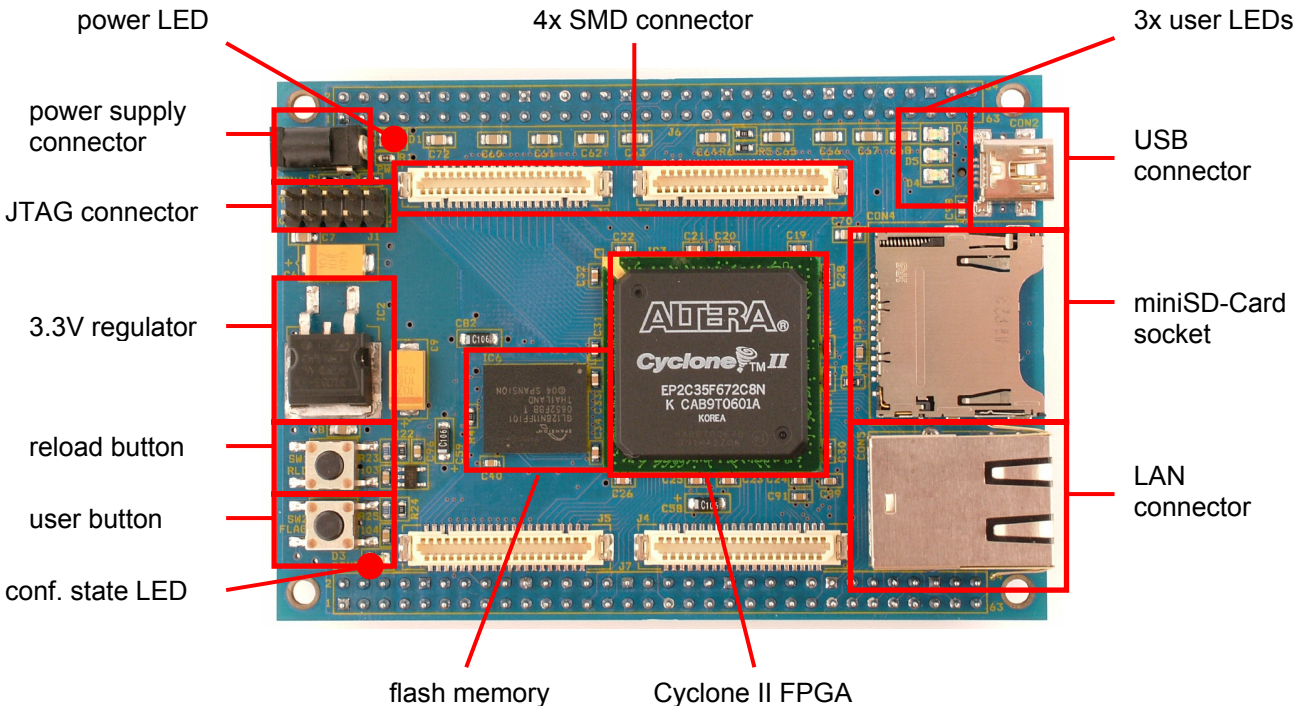
- Small size of the FPGA board (only 96x68 mm) makes it possible to use it in the end application as a daughter board,
- 172 Cyclone II I/O pins are *exclusively* available at the expansion connectors,
- More than a half of these I/Os are connected to common connectors with 2.54 pitch and high duty gold plated precision contacts,
- Two controllers for the world most used data buses (Ethernet and USB) already soldered on FPGA board,
- One SODIMM SDRAM memory socket for up to 256 Mbytes SDRAM module,
- 16 Mbytes flash memory,
- Integrated power conditioning.

Description of the FPGA board

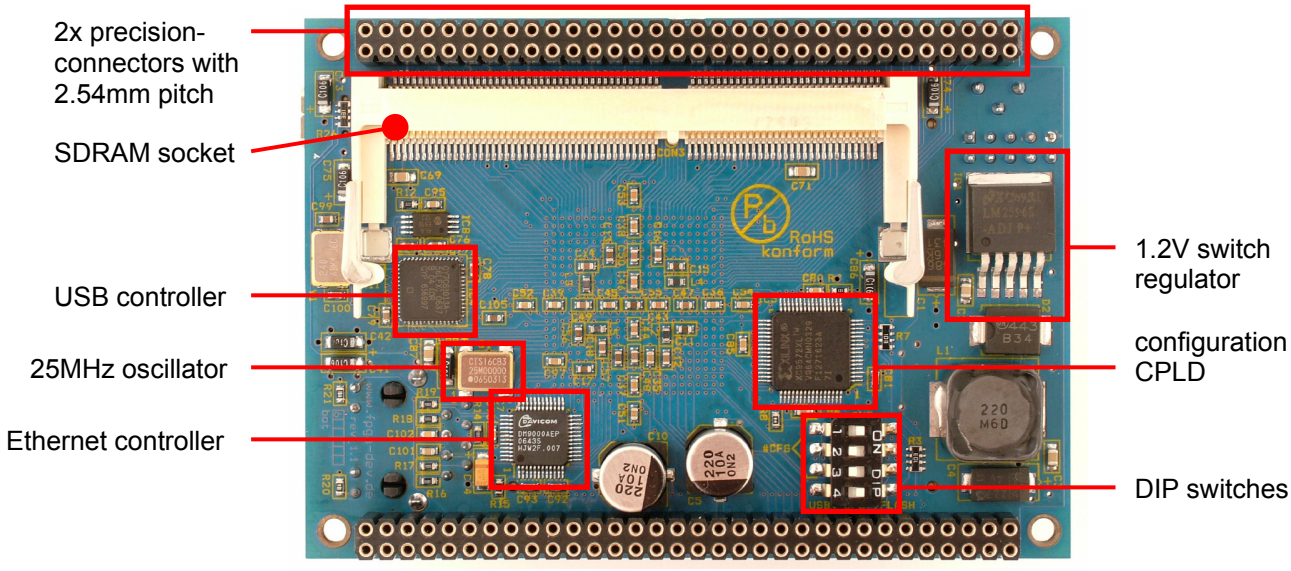
Block diagram



FPGA board components - top side



FPGA board components - bottom side



Altera Cyclone II FPGA

The used Altera Cyclone II FPGA EP2C35F672C8N contains in total 33,216 LE (LE=LUT+DFF), 483 kbit memory, 35 embedded multipliers and 4 PLLs.

Configuration CPLD

The CPLD can configure FPGA with one of 8 selectable configuration files, which can be programmed into flash memory.

Flash memory

The 16 MByte large flash memory device can hold up to 8 FPGA configuration files and application specific data. The flash device is connected through 16 bit wide data bus to FPGA.

miniSD-Card socket

Flash cards for the miniSD-Card Socket are available today with capacities up to 4 GByte.

SDRAM memory socket

SODIMM socket accepts laptop SDRAM memory modules with capacity up to 256 MByte. The data bus to the FPGA is 64 bit wide, which results in 1 GByte/sec maximum total data rate.

USB controller

The integrated high speed USB controller CY7C68013 communicates with 480Mbits/sec with a PC or another proper USB host. Preprogrammed E²PROM already contains firmware for 8051 based microcontroller of the CY7C67013. The firmware configures the endpoints as follows:

endpoint	direction	FIFO count x block size
EP2	out	2 x 512 Byte
EP4	out	2 x 512 Byte
EP6	in	2 x 512 Byte
EP8	in	2 x 512 Byte

The general programmable interface of USB controller (FPGA↔USB) is configured as 16 bit wide slave FIFO interface. The FIFO interface is clocked with 25 MHz, which allows net transfer of 50 Mbyte/sec. between FPGA and USB controller.

The firmware-programmed vendor and product IDs are reserved for development intentions only:

idVendor	0x04B4
idProduct	0x1004

You *must* change these IDs if you use the FPGA board as a part of a commercial product!

You can use delivered FPGA configuration tool for FPGA configuration over USB interface without any JTAG adapter.

Ethernet controller

The FPGA board provides 100/10MBit Ethernet support via Davicom DM9000A Ethernet controller chip. This makes in fact a very simple and FPGA logic resources saving connection to Ethernet networks possible.

Crystal oscillator

The 25 MHz reference clock is generated by crystal oscillator Q1. This clock signal is provided to FPGA, FIFO interface of USB controller and Ethernet controller. The usage of a reference clock makes sure, that all components can communicate with FPGA absolutely synchronous in one single clock domain.

User I/O

A debounced push button can be used for direct user input detection. The released user button is identified by logic low (0 volt) and pressed one by logic high (3.3 volt).

For simple outputs three user LEDs are provided on the FPGA board. Each LED is driven directly by a pin of the FPGA. Driving related pin to a logic low (0 volt) turns the LED on.

Reload button

Pushing the reload button (SW1) clears the configuration data inside FPGA. Immediately after releasing the reload button the FPGA is reconfigured by CPLD with a configuration contained in flash if the DIP switch (4) in the **ON** position.

Expansion connectors

User circuits can be connected to FPGA through two expansion connectors on the bottom of the board (J6 and J7 with 2.54 mm pitch) and through four surface mounted connectors on the top of the board (J2-J7). Four different signal types are available at expansion connectors:

1. FPGA-I/Os - FPGA in- and outputs, the signal direction is application specific and defined by the user,
2. FPGA-I/Os or PLL output - same as type one, additionally these pins can be used as PLL clock output,
3. FPGA- or PLL clock inputs - input only FPGA pins, allow direct clock sourcing to PLL circuits,
4. Power supply connectors - +5V, +3.3V and power ground.

The following table lists the availability and count of the first three pin types at different expansion connectors:

conn. / signal type	1	2	3
J2	20	0	1
J3	20	0	1
J4	19	1	1
J5	21	0	0
J6	43	0	1
J7	42	1	1
Σ	165	2	5

Note: All these 172 FPGA I/Os are *exclusively* available at expansion connectors, they are *not shared* with any other FPGA board device or circuit.

Power supply

The FPGA board is power supplied through the CON1 connector. The centre of the power supply plug must be positive (+5 volt) and the barrel must be negative (ground). As an alternative, you can use power pins 2, 4 (both positive) and ground pins of expansion connector J6 to supply power to the FPGA board. The power supply must provide a regulated voltage of 5 volt (±10%, min. 1 ampere).

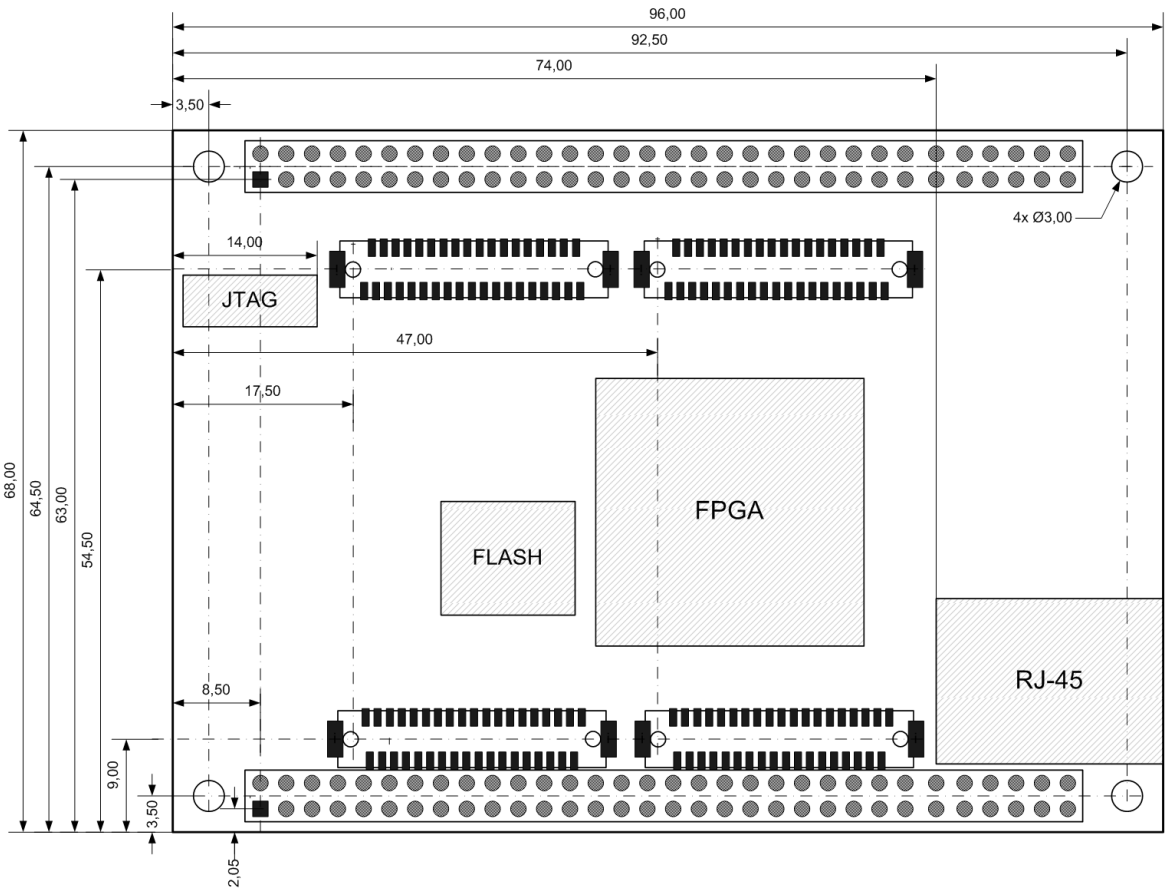
The FPGA Board components require either 1.2 volt supply (FPGA core) or 3.3 volt supply (FPGA-I/Os, SDRAM, USB, Ethernet, flash, etc.). These voltages are provided by a high efficient switch regulator (1.2 volt) and linear regulator (3.3 volt). Both regulators deliver currents up to 3 ampere.

The real current requirement depends on the following factors:

- Configuration loaded into FPGA,
- SDRAM memory usage,
- Current drawn by user expansion circuits supplied through FPGA board.

Important: There is no power supply reverse-polarity protection circuit on FPGA board! Wrong power supply polarity *will* damage FPGA board components!

Physical dimensions and expansion header positions



All dimensions are in millimetres

Setting-up operations

FPGA design software

Altera Cyclone II EP2C35 FPGA is supported by the free Altera Quartus II Web Edition design software. Please visit www.altera.com for further information and download.

USB drivers installation

Install Cypress USB drivers before using the FPGA board USB interface. Execute the „~\usb\SETUP_FX2LP_DVK_1004.exe“ for installation. Many tools, firmware examples and documents needed for successful and fast development of own CY7C68013 firmware and PC applications are installed too.

FPGA pin allocation file

All pin allocations of the FPGA are contained in „~\fpga\pin_assignments.qsf“.

FPGA configuration

You can configure the Cyclone II FPGA in three different ways:

- Via USB interface,
- With content from the flash memory,
- Via JTAG interface.

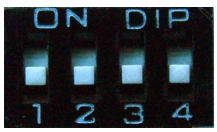
Let’s have a look on every of these possibilities.

FPGA configuration via USB interface

As earlier mentioned, the E²PROM is preprogrammed with a small firmware for the 8051 MCU of the USB controller. This firmware uses internal endpoint 1 for FPGA configuration data reception. After reception, the configuration data is shifted by 8051 MCU in serial manner (PS mode) into FPGA.

Please follow the lower instructions for the FPGA configuration via USB:

1. Shove DIP switch (4) in **OFF** position:



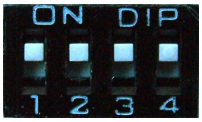
2. Clear current configuration by pressing reload button,
3. Connect PC and FPGA board through USB cable,
4. Start FPGA configuration tool,
5. Choose the raw bit configuration file (*.rbf).

The configuration procedure starts immediately after file selection dialog is closed and lasts about 5 seconds. A success message confirms finished FPGA configuration. At the same time the yellow LED turns on.

Note: Once FPGA configuration procedure starts, await a success or failure message before next attempt.

FPGA configuration from the flash memory

The flash memory can contain up to 8 selectable configuration files for standalone FPGA configuration. The configuration starts after the power supply is applied to the FPGA board and the highest DIP switch (4) is in **ON** position. The lower DIP switches (1..3) determine address range in the flash memory which is used for loading configuration data. The loaded configuration data is shifted in serial manner into FPGA (PS mode). The lower 8 MByte of flash memory are segmented in address ranges as follows:

# configuration	address range	switch position
0	0x00.0000-0x0f.ffff	
1	0x10.0000-0x1f.ffff	
2	0x20.0000-0x2f.ffff	
3	0x30.0000-0x3f.ffff	…
4	0x40.0000-0x4f.ffff	…
5	0x50.0000-0x5f.ffff	…
6	0x60.0000-0x6f.ffff	…
7	0x70.0000-0x7f.ffff	

Each memory segment is large enough for storage exactly one FPGA configuration. Unused segments can be used for any other purposes.

Note: Configure the FPGA from the flash memory only when a flash segment with a valid configuration data is selected!

FPGA configuration via JTAG

The pin configuration of JTAG connector complies with the Altera specifications. You can use both the original Altera USB Blaster and the compatible one from terasIC. (www.terasic.com.tw).

Note: The usage of a JTAG adapter is the only way to:

- In circuit debugging of a NIOS II system,
- Using the Signal Tap II logic analyzer,
- Programming flash memory.

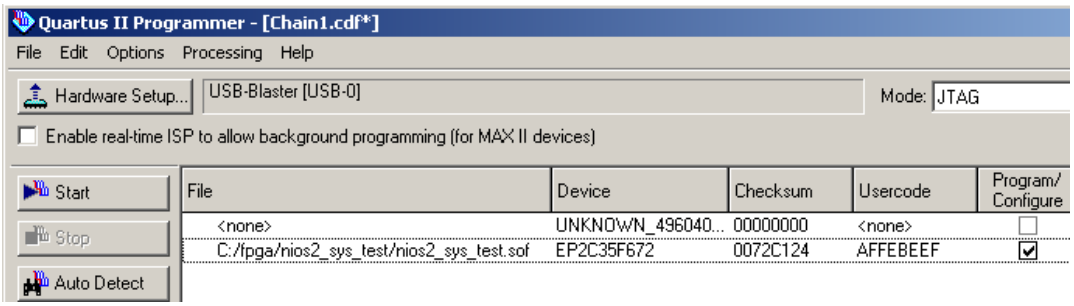
JTAG chain

The JTAG chain carried out at JTAG connector consist of Xilinx configuration CPLD and Altera Cyclone II FPGA. The configuration CPLD is already programmed; there is no need for any modifications of its function. If you use a JTAG adapter in conjunction with Altera Software please note: The Altera Software reports the configuration CPLD as an unknown device. It's not a malfunction or a bug; it does not impact usage of Altera Software!

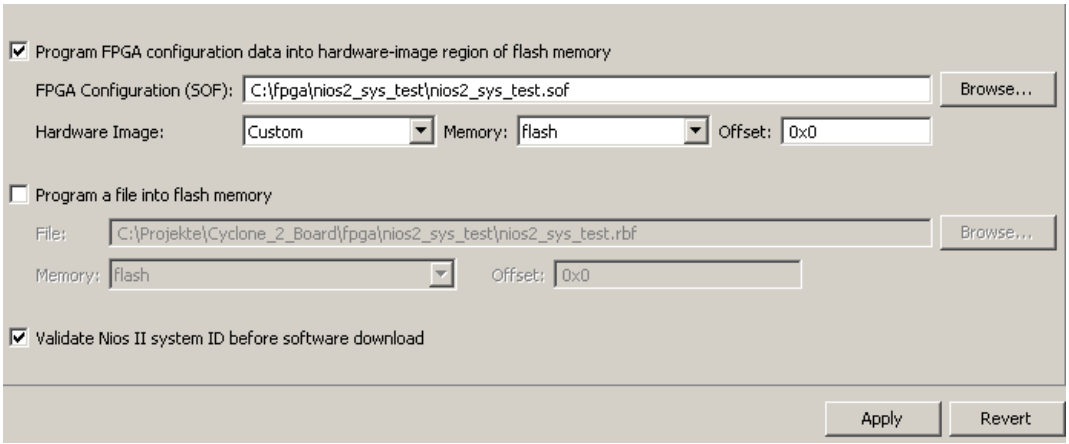
Flash memory programming

The programming of flash memory requires a JTAG adapter, a working NIOS II design (contained in „~\fpga\nios2_sys_test\...“) and installed NIOS II IDE Software. Following steps have to be done to program the flash memory with a configuration file at address 0x0:

1. Start "Quartus II Programmer" application from NIOS II IDE
   (Tools→Quartus II Programmer)
2. Configure FPGA with „~\fpga\nios2_sys_test\nios2_sys_test.sof“ file
   (Auto Detect→double click at file field of EP2C35→Select file→Start)



3. Start „Flash Programmer“ application from NIOS II IDE *(Tools→Flash Programmer)* and select the desired FPGA configuration file and destination address range (offset):



4. Push „Program Flash“. The Flash Programmer window will automatically close. All output messages will appear at console window of NIOS II IDE.

NIOS II – example SOPC system

The enclosed CD contains an example NIOS II system for Quartus II v7.2 (CDROM path „~\fpga\nios2_sys_test\...“). This example system was developed to check the function of all components contained at the FPGA board. The results of the check subroutines are indicated via the user LEDs. The top level entity file of the example NIOS II system is „~\fpga\nios2_sys_test\top_level.vhd“

Memory test

Memory test tests the connection and integrity of flash and SDRAM memories. For a successful SDRAM test insert a 256 MByte memory module into SDRAM socket. The user LED 1 (D4) turns on, if SDRAM test succeeds. The user LED 2 (D5) indicates a succeeded flash memory test.

Note: Memory test erases all contents in flash and SDRAM memory!

Ethernet test

After Ethernet controller initialisation every received data package generates a processor interrupt. The interrupt service routine reads the Ethernet packet data from DM9000A and sends its content immediately back to sender. Every call of interrupt service routine changes the state of the user LED 3. The target IP address of the Ethernet controller is set by initialisation routine to „**01.60.6E.11.02.0F**“.

Note: You can use Ethernet packet sniffer and generator like **CommView** from **TamoSoft** to generate and receive Ethernet packets.

USB test

A VHDL component is instantiated in NIOS II example system for USB controller test. This component is not connected to NIOS II example system. It consist of two 512 Byte large FIFOs and realises a simple echo application. One FIFO serves endpoints EP2 and EP6, the other EP4 and EP8. Content of packets received through EP2 endpoint is read via FIFO interface and stored in assigned FIFO. After that, the data is send back through EP6 endpoint. The same procedure is applied to endpoints EP4 and EP8.

Note: You can test the quality of the USB connection with Cypress tool **CyBulk**.

CD content

~\cpld\...	- configuration CPLD programming file
~\data_sheets\...	- data sheets of used components
~\docs\...	- this file
~\fpga\...	- IP component for connection of Ethernet controller to NIOS II - FPGA pin allocation file
~\fpga\nios2_sys_test...	- NIOS II example system
~\usb\...	- USB drivers and documentations of Cypress USB controller
~\usb\firmware\...	- firmware sources of USB controller
~\usb\programmer\...	- source codes of Windows FPGA programming tool
~\usb\programmer\Release\...	- Windows FPGA programming tool

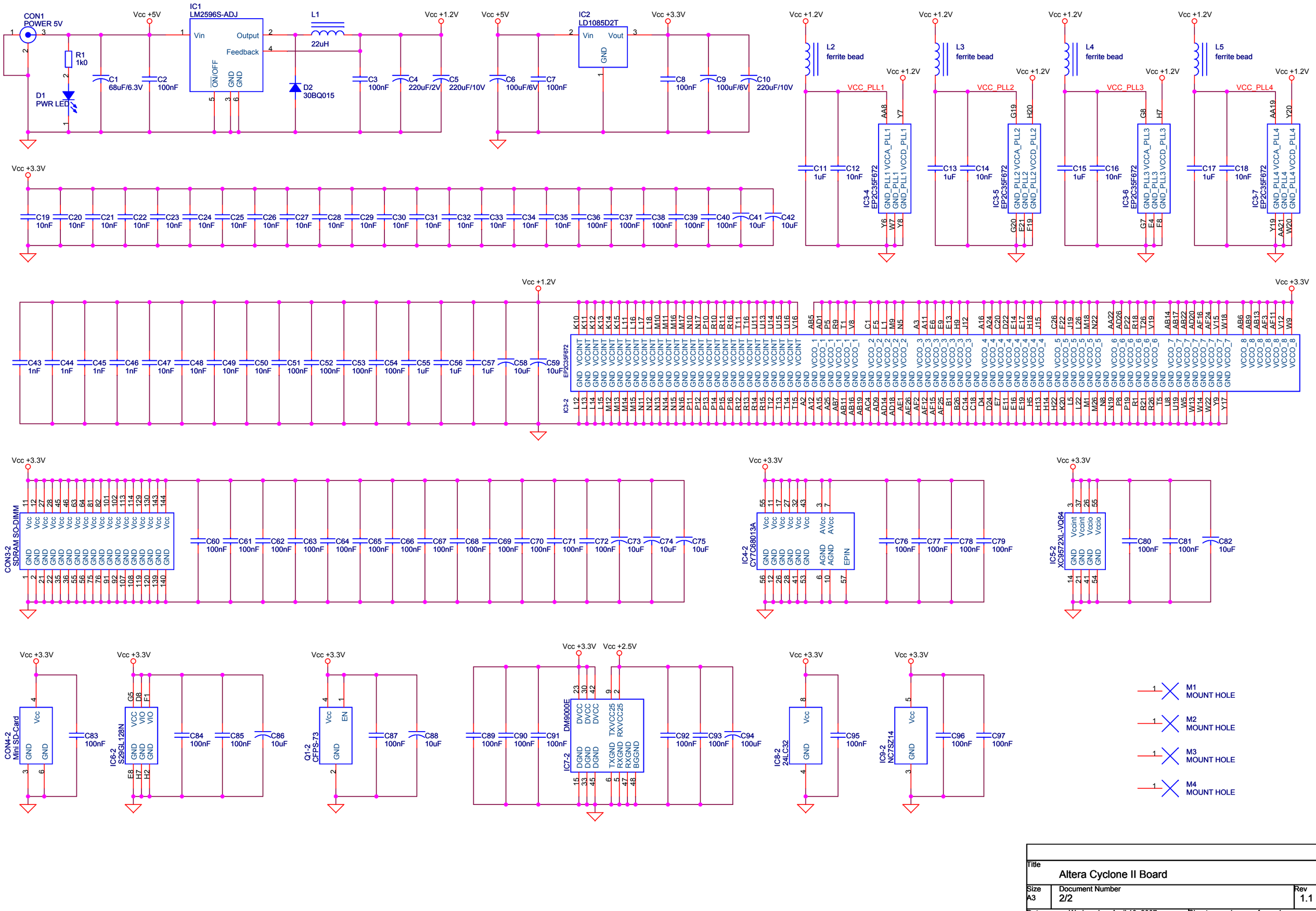
Document revisions and changes

revision / date	Changes
1.00 / 10.11.2007	initial version

Trademarks

Cyclone II, NIOS II, Signal Tap II and Quartus II are trademarks of Altera Corporation.
CyBulk is a trademark of Cypress.
ComView is a trademark of TamoSoft.

Schematics and component diagrams


CON1
POWER 5V
R1
1k0
D1
PWR LED
C1
68uF/6.3V
C2
100nF
IC1
LM2596S-ADJ
Vin
Output
Feedback
ON/OFF
GND
GND
L1
22uH
D2
30BQ015
C3
100nF
C4
220uF/2V
C5
220uF/10V
C6
100uF/6V
C7
100nF
IC2
LD1085D2T
Vin
Vout
GND
C8
100nF
C9
100uF/6V
C10
220uF/10V
Vcc +5V
Vcc +1.2V
Vcc +3.3V
L2
ferrite bead
L3
ferrite bead
L4
ferrite bead
L5
ferrite bead
VCC_PLL1
VCC_PLL2
VCC_PLL3
VCC_PLL4
C11
1uF
C12
10nF
C13
1uF
C14
10nF
C15
1uF
C16
10nF
C17
1uF
C18
10nF
IC3-4
EP2C35F672
IC3-5
EP2C35F672
IC3-6
EP2C35F672
IC3-7
EP2C35F672
GND_PLL1 VCCA_PLL1
GND_PLL1
GND_PLL1 VCCD_PLL1
GND_PLL2 VCCA_PLL2
GND_PLL2
GND_PLL2 VCCD_PLL2
GND_PLL3 VCCA_PLL3
GND_PLL3
GND_PLL3 VCCD_PLL3
GND_PLL4 VCCA_PLL4
GND_PLL4
GND_PLL4 VCCD_PLL4
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100nF
C54
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1uF
C56
1uF
C57
1uF
C58
10uF
C59
10uF
IC3-2
EP2C35F672
VCCINT
GND
VCCO_1
VCCO_2
VCCO_3
VCCO_4
VCCO_5
VCCO_6
VCCO_7
VCCO_8
C60
100nF
C61
100nF
C62
100nF
C63
100nF
C64
100nF
C65
100nF
C66
100nF
C67
100nF
C68
100nF
C69
100nF
C70
100nF
C71
100nF
C72
100nF
C73
10uF
C74
10uF
C75
10uF
CON3-2
SDRAM SO-DIMM
IC4-2
CY7C68013A
C76
100nF
C77
100nF
C78
100nF
C79
100nF
IC5-2
XC9572XL-VQ64
C80
100nF
C81
100nF
C82
10uF
CON4-2
Mini SD-Card
C83
100nF
IC6-2
S29GL128N
C84
100nF
C85
100nF
C86
10uF
Q1-2
CFPS-73
C87
100nF
C88
10uF
IC7-2
DM9000E
C89
100nF
C90
100nF
C91
100nF
C92
100nF
C93
100nF
C94
100uF
IC8-2
24LC32
C95
100nF
IC9-2
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C96
100nF
C97
100nF
M1
MOUNT HOLE
M2
MOUNT HOLE
M3
MOUNT HOLE
M4
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IC6-1
S29GL128N

CON3-1
SDRAM SO-DIMM

IC4-1
CY7C68013A

IC8-1
24LC32

MINI USB CON2

CON4-1
Mini SD-Card

Q1-1
25MHz

Y1
24MHz

IC7-1
DM9000E

CON5
RJLBC-060TC1

SW3
SW DIP-4

SW1
RELOAD

SW2
FLAG

IC5-1
XC9572XL-VQ64

BLOCK_1

BLOCK_2

BLOCK_3

BLOCK_4

IC3-3
EP3C39F672

J1
JTAG

IC3-1
EP3C25F672

J2
VESA CON 41

J3
VESA CON 41

J4
VESA CON 41

J5
VESA CON 41

J6
RM 2.54

J7
CONN PLUG 32x2

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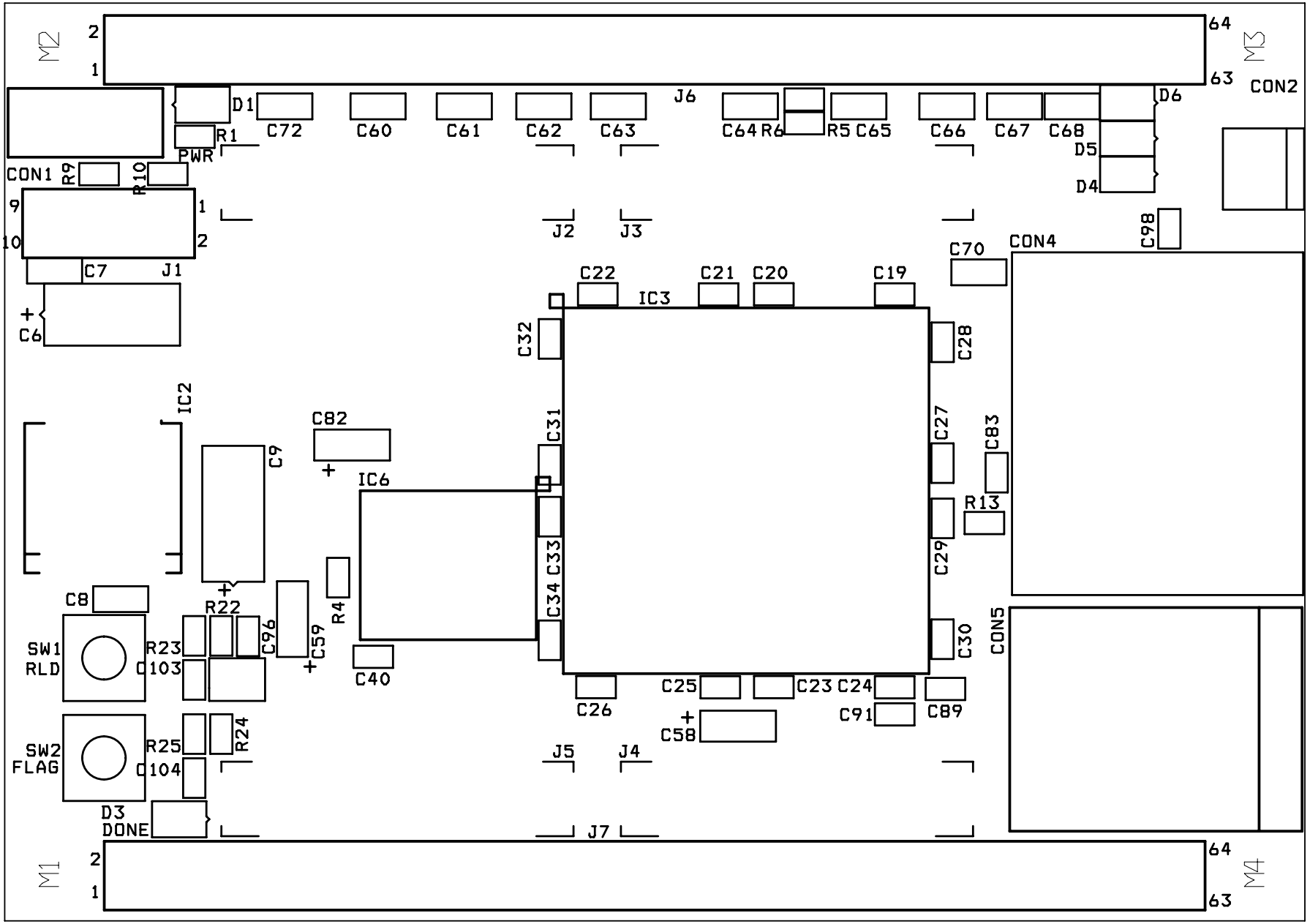
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2
1
64
63
M3
CON2
D1
R1
PWR
C72
C60
C61
C62
C63
J6
C64
R6
R5
C65
C66
C67
C68
D6
D5
D4
CON1
R9
R10
9
10
1
2
J2
J3
C98
C70
CON4
C7
J1
C6
C22
C21
C20
C19
IC3
C32
C28
IC2
C82
C31
C27
C83
C9
IC6
R13
C33
C29
C34
R4
C8
R22
C96
C59
C30
CON5
SW1
RLD
R23
C103
C40
C25
C23
C24
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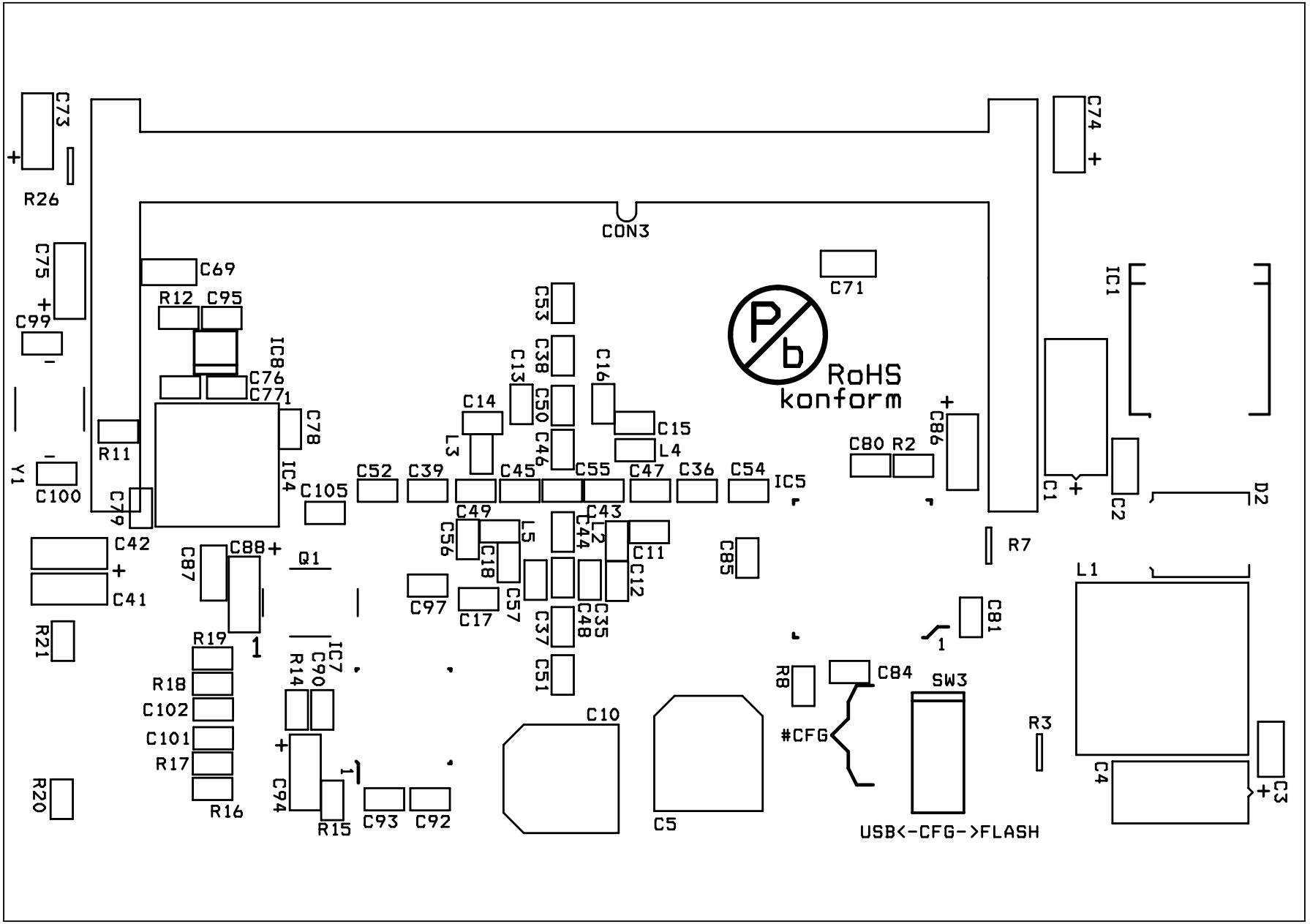
R25
R24
C104
J5
J4
D3
DONE
J7
M1
M4


C73
R26
C74
CON3
C75
C99
C69
R12
C95
IC8
C76
C771
C78
R11
IC4
C79
C100
Y1
C105
C52
C39
C45
C55
C47
C36
C54
IC5
C53
C38
C13
C50
C46
C14
L3
C16
C15
L4
C71
RoHS
konform
C86
C80
R2
IC1
C1
C2
D2
C49
C56
L5
C18
C43
C44
L2
C11
C12
C85
R7
C42
C41
C88
C87
Q1
C97
C17
C57
C37
C48
C35
C51
L1
C81
R21
R19
R18
C102
C101
R17
R16
IC7
R14
C90
C94
R15
C93
C92
C10
C5
R8
C84
SW3
#CFG
R3
C4
C3
R20
USB<-CFG->FLASH